Project Report:

Analog to Digital Conversion by Successive Approximation

EGR 334: Analog-Digital Interface
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Abstract

The goal of this project is to make a Successive Approximation Register (SAR) Analog to Digital Converter (ADC). This will be achieved by creating an 8-bit SAR logic network using Microchips 7474 D-Type Flip Flops. The logic network will then be paired to a R2R DAC (Digital Analog Converter) that feeds into a LM741 comparator.

Introduction

The end ambition for this project is to create a SAR ADC. There will be 3 main parts to the SAR ADC constructed for this project. First is the Successive Approximation Register (SAR), and is what takes our analog input and turns it into a digital representation through a binary search of all possible configuration levels. It then converges to a specific digital output. Through the use of D-Type Flip Flops it is possible to create the sort of logic needed for this operation. The second integral part of a completed SAR ADC is the Digital to Analog Converter (DAC) that takes the outcoming bits from the SAR Logic Network and converts the output back to an analog signal that is then sent to a comparator. We are using a R2R DAC network to accomplish this necessary part of the system. Lastly is the Analog Voltage comparator, this small circuit is what compares the outcoming DAC signal to the Vin of the system. The comparator then outputs the result of these comparisons to the SAR Logic Network. These three circuits all work together to create the SAR ADC system for this project. To complete this project it will be operated in the following way:

- Research SAR's
- Understand the support circuits needed for a SAR ADC
- Source needed parts for SAR ADC
- Create and Demonstrate 4-Bit SAR ADC
- Create and Demonstrate 8-Bit SAR ADC

Scope

For this project a Circuit was created that takes and analog input Vin and outputs its digital Signal in the form of Bits. The original goals of this project were as follows:

- To understand the different Types of ADC's.
- To discover how a SAR works.
- To create a SAR based ADC.
- To demonstrate the SAR ADC Built for this project.

Objectives

The objective of this project was to understand how to SAR ADCs function and to then create a SAR ADC. The Steps to achieve this are as follows:

- Create a SAR logic network with D-type flip flops.
- Create a SAR ADC System.
- Demonstrate a working 4-Bit SAR ADC
- Demonstrate a working 8-Bit SAR ADC

Challenges

- There's a lack of resources on how to successfully wire a 8-bit ADC using D-type flip flops.
- Most source material is at a PhD level and for CMOS Chip Creation.
- The circuit contains a heavy amount of wiring, making debugging difficult.
- SN74LS74AN D-type flip flops are prone to burning out, and it is unclear when they do so. It is also difficult to identify which is burnt out, especially when using many of these chips.
- The team had less time than what is ideal due to other projects and responsibilities.

Hardware Requirements

Texas Instruments SN74LS74AN

The SN74LS74AN is the main component used for this project as it is essential in creating the Successive Approximation Register circuit. The part is made by Texas Instruments and Sells at 58 cents per piece. The component has two positive edge triggered d-type flip flops

Figure 1: SN74LS74AN [4]

Features of SN74LS74AN:

- Two Positive Edge Flip Flops
- Multiple package sizes
- Dependable

Analog Discovery 2

Digilent Analog Discovery 2 is a USB oscilloscope and multi-function instrument that allows users to measure, visualize, generate, record, and control mixed-signal circuits.

Figure 2: Analog Discovery 2

(www.digilent.com)

Features of Analog Discovery 2:

- Two-channel USB digital oscilloscope
- Two-channel arbitrary function generator

- Stereo audio amplifier to drive external headphones or speakers with replicated AWG signals
- 16-channel digital logic analyzer (3.3V CMOS and 1.8V or 5V tolerant, 100MS/s)
- 16-channel pattern generator (3.3V CMOS, 100MS/s)
- 16-channel virtual digital I/O
- Two input/output digital trigger signals for linking multiple instruments (3.3V CMOS)
- Single channel voltmeter (AC, DC, ±25V)
- Network Analyzer – Bode, Nyquist, Nichols transfer diagrams of a circuit. Range: 1Hz to 10MHz
- Spectrum Analyzer – power spectrum and spectral measurements
- Data Logger - Exportable data and plot functionality
- Impedance Analyzer - Capacitive and Inductive Elements
- Protocol Analyzer - SPI, I2C, UART, and CAN
- Two programmable power supplies

LM741 Op-Amp

The LM741 is a general purpose operational amplifier.

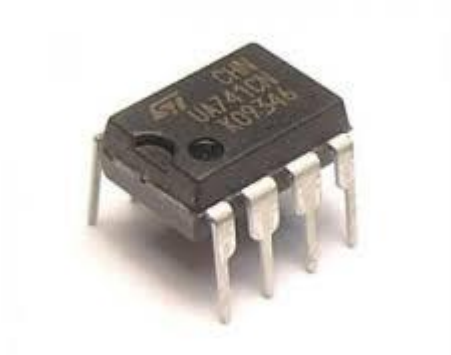


Figure 3: The LM741. [3]

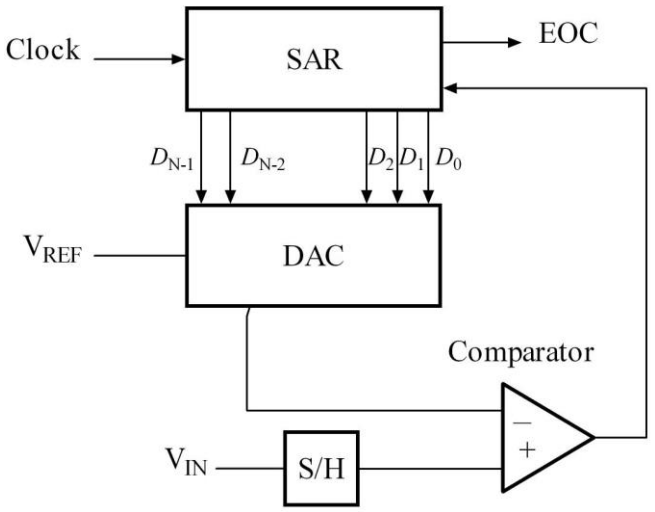
Features:

- Overload Protection on input and output
- No latchup when the common mode range is exceeded

Project Description

Overview

Many analog-digital converters work by having a successive approximation register (SAR) digitally approximate (guess) a voltage, and having an op-amp comparator compare the guessed voltage to the analog input. The output of the comparator tells the SAR whether to increase or decrease it's guessed voltage. A block diagram for a SAR ADC is shown on the right.



The SAR's "guess" begins at 0v (binary: 0000). The DAC turns this into an analog voltage (0v), and a comparator compares it to the input voltage (from the sample/hold network; not included in project). The comparator feeds back into the SAR, telling it whether to increase or decrease it's guessed value (between 0000, and 1111).

For the purposes of this project, the sample/hold network is omitted due to a relatively constant input voltage from a potentiometer. A four-bit ADC will be designed to digitally represent the voltage (between 0 and 5v) as a number between 0 and 16. This four-bit ADC will consist of three primary subcomponents: the successive approximation register (SAR), the digital-analog converter (DAC), and the op-amp comparator.

SAR Logic Network

The SAR is first initialized so that the most significant bit is equal to digital 1. This is then given to DAC, which will then supply the analog equivalent of the digital signal. Into the comparator circuit to be compared to the sampled input voltage. If this analog voltage is greater than Vin the comparator causes the SAR to reset this bit, otherwise its left as a 1. The next bit is then set 1 and the same process is repeated. It continues this test

until every bit in the SAR is done. The Bits that result from this are the digital representation of the Analog sampled signal (Vin) they are then outputted by the SAR at the end of conversion (EOC).

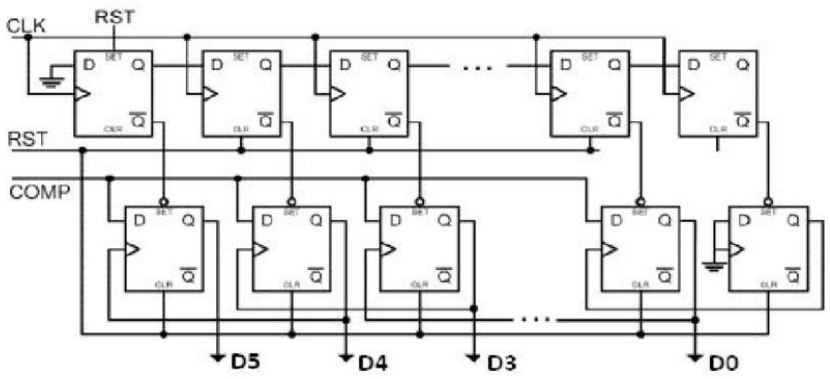


Figure 4: SAR D-type Flip Flop [2]

DAC

Digital-analog conversion is done using a resistor ladder (known as an R-2R network, for visually-evident reasons). The idea behind this type of network is that a voltage divider is created between each bit and ground, effectively dividing the voltage at higher levels for more-significant bits. As bits are enabled, the output voltage, V_{out} is increased. This resistor arrangement allows for the conversion of a four-bit digital signal into an analog voltage between 0v and the logic high (5v).

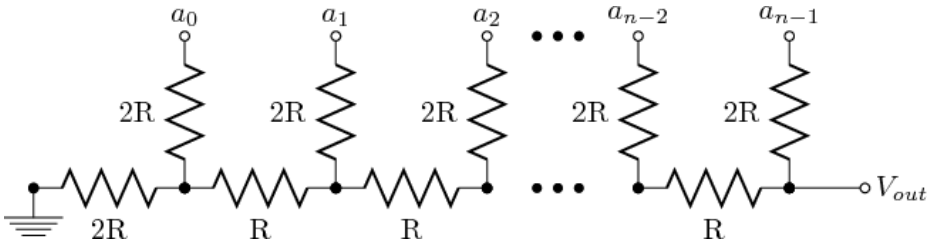


Figure 5: R2R DAC

As an input, the DAC takes 5v digital TTL logic from the D-type flip-flops in the SAR. The R2R allows more significant bits to yield more voltage than less significant bits. The advantage of an R2R network over comparable digital-to-analog alternatives is that all the resistor values are the same. This makes the parts cheaper as the resistance value does not matter so long as they are the same.

Comparator

The comparator takes in the analog output of the DAC and the input signal. It compares the two and then outputs a value to the SAR, indicating to the SAR whether to increase or decrease it's approximated voltage.

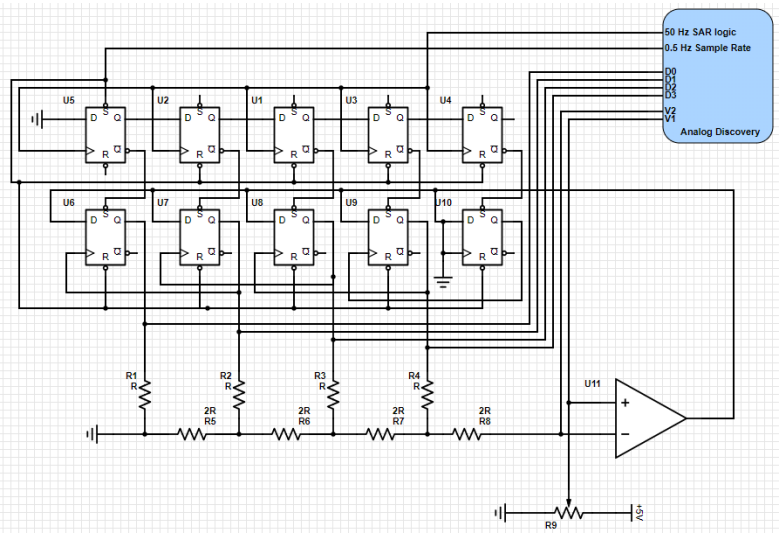
Because a comparator is essentially a default function for op-amps, not much setup is required. The op amp receives V_{ref} from the DAC, and compares it to the input voltage from the potentiometer. Depending on the output from the comparator, feedback is sent to the SAR whether to increase or decrease its approximation.

Future Enhancements

This project gave us countless issues when it came to wiring up the SAR ADC's. To avoid this problem we would highly recommend the usage of PCB's to control the wiring setup of this project. Reliability of the 7474 Flip Flops also caused us much distress. We believe using a more reliable Flip Flop would greatly help in the creation, testing and maintaining of these SAR ADC circuits. It is Also our recommendation that more class time is allocated to working on these projects. Another way to enhance the project would be to introduce a way to read the values in the SAR in a way that ensures that the values are accurate. The current system is continuously tuning, so a way to pause it long enough to read a value would be nice.

Conclusion

To test the SAR ADC, initially, 8 bits were used (for a total of 18 D-flip flops), however to simplify the project due to time constraints, this was reduced down to four bits (for a total of 10 D-flip flops).

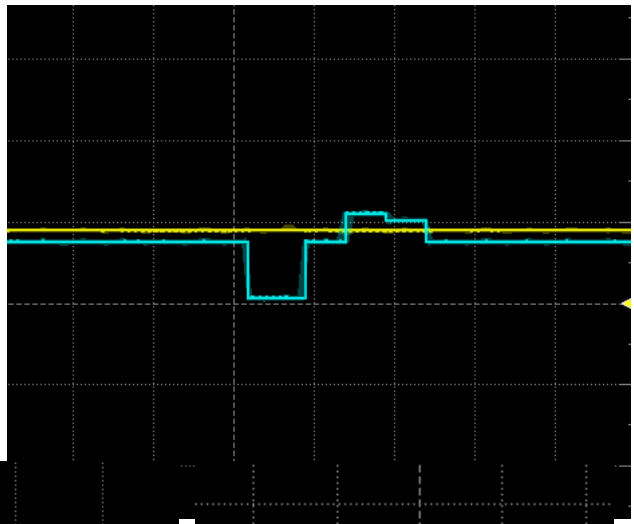


The schematic shown on the right was constructed using an LM741 op-amp, and SN74LS74 D type flip-flops. The analog discovery was used to provide clock signals for the sample rate and the digital logic.

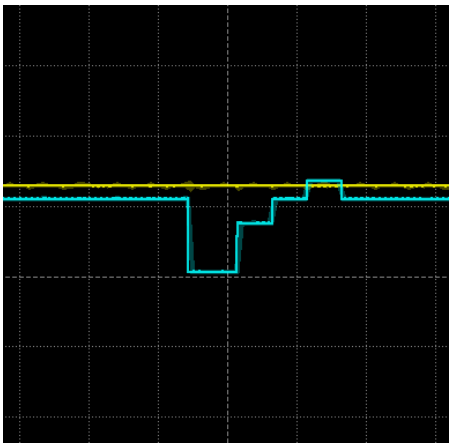
Ideally, the SAR network should begin guessing voltages once the sample rate clock is triggered (rising edge). From there, the SAR should guess several voltages until it finds the voltage corresponding to a binary number that is closest to the input voltage.

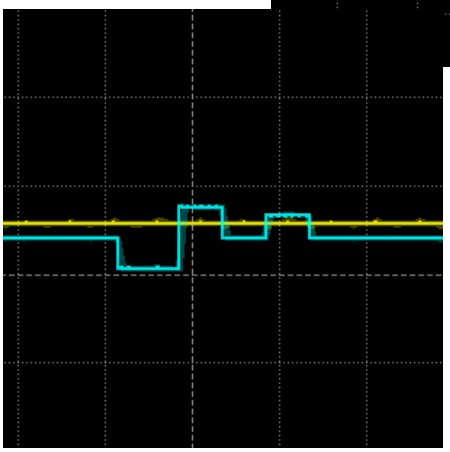
With the analog discovery connected to the potentiometer on one input, and the output of the DAC to the other, as the potentiometer is turned, the SAR should visibly guess the output voltage.

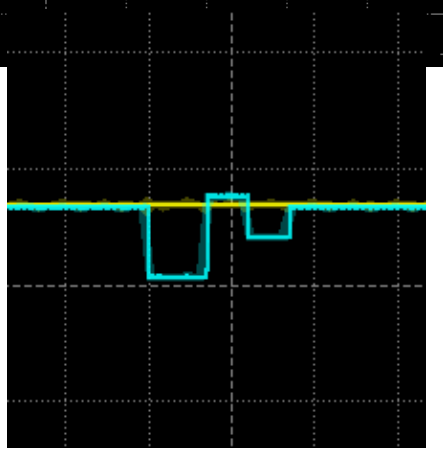
This output can be seen in the waveform on the right. The yellow voltage corresponds to the analog input, while the blue voltage corresponds to the voltage guessed by the SAR. In the image on the right, the potentiometer was turned to a setting corresponding voltage of approximately 1.8v (yellow). Each step shown in blue represents the SAR guessing a new voltage.



The work of the ADC can be seen as it guesses different voltages. Several are shown below:

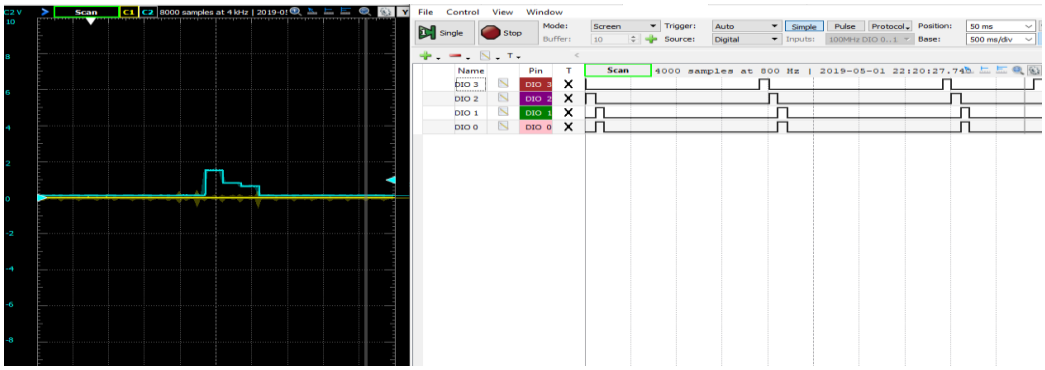




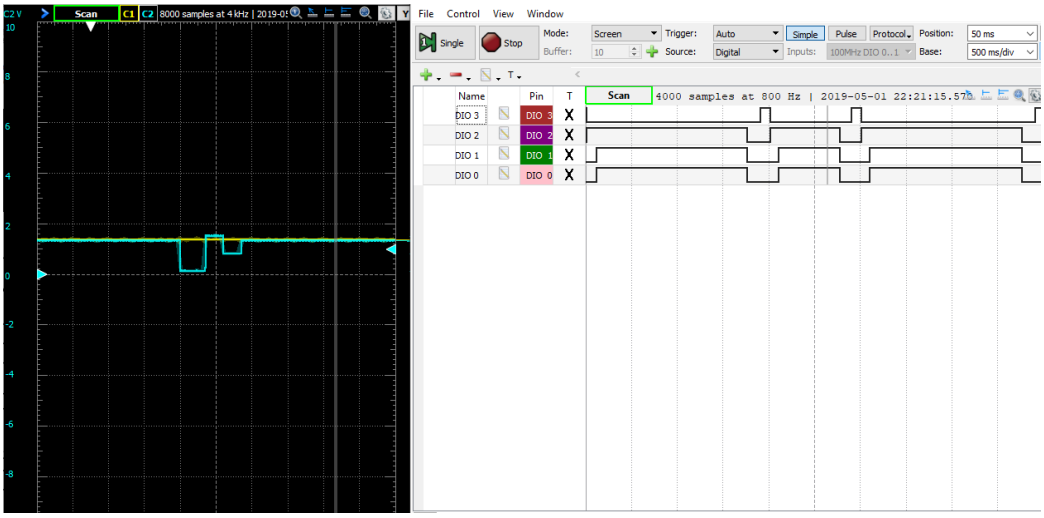


The digital logic can also be examined using the analog discovery. The analog discovery was connected to the digital logic pins of the ADC (SAR output). The final binary number corresponding to the guessed voltage can be seen across digital pins 0 through 3. Shown below are several examples.

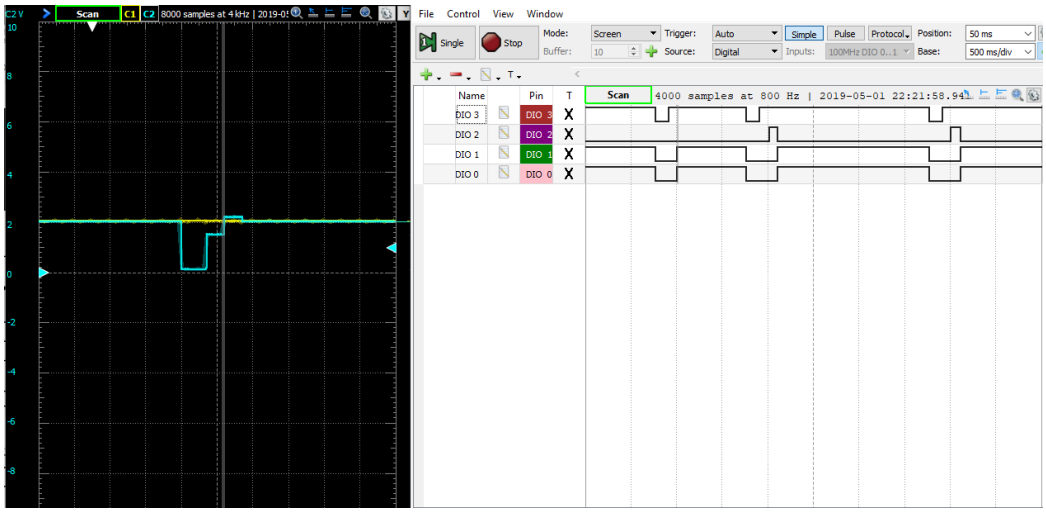
SAR approximation of minimum voltage (logic 0000)



SAR approximation of 1.5v (logic 0111)



SAR approximation of 2.0v (logic 1011)



To illustrate this effect visually, LEDs can be connected to the digital output pins of the SAR. The LED output can be observed (LSB to MSB) at the voltages below: