FINAL REPORT

FM Demodulation Using a Phase-Locked Loop

EGR 330 (DESIGN OF ELECTRICAL SYSTEMS)
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Table of Contents

Table of Figures

Abstract

This project has the main objective of building an example phase lock loop. The system will consist of a phase detector which is in a feedback loop with a variable frequency oscillator. The phase detector will compare the signal generated by the oscillator with the phase of the input periodic signal, with the purpose of keeping the phases matched. This will allow us to use the system for demodulation as the phase-locked loop is capable of tracking an input frequency as well as generate a frequency consisting of multiples of the input frequency. Demodulation can then be used to recover information contained in the modulated carrier wave such as FM demodulation networks for FM operation.

Introduction

Phase-Locked Loops (PLLs) are widely used in technologies that require motor speed controls, tracking filters, frequency synthesis providing multiple of a reference signal frequency, and frequency shift keying or FSK that decodes for demodulation carrier frequencies. For our project, we will be using a phase-locked loop to demodulate an existing frequency modulated signal. This can be done by allowing the PLL to lock onto the frequency of an input waveform. This is accomplished through the use of a phase detector, a low-pass filter or also known as a loop filter, and a voltage-controlled oscillator (VCO). All of which are combined into a negative-feedback system as shown below in figure 1.

Negative-feedback system:

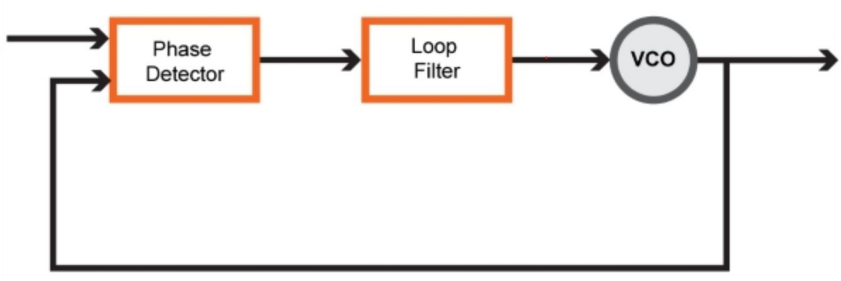

Figure 1: PLL Negative Feedback

Once the PLL has successfully locked it will produce an output sinusoid that exactly mirrors the input voltage. Do to our application of FM demodulation, the output sinusoid with the same frequency as the input signal isn't particularly useful. We will instead be using the output from the loop filter as the demodulated signal. This can be summarized:

- The phase detector produces a signal proportional to the phase difference between the output of the voltage-controlled oscillator and the input waveform.
- The loop filter reduces the noise of the signal for the voltage-controlled oscillator.
- The signal then becomes the control signal for the voltage-controlled oscillator.

The voltage controlling the VCO must oscillate with the same frequency as the originally modulated waveform, and this output can be taken as the FM demodulated output.

Scope

Background: Frequency Modulation

Analog information such as sound pressure (an audio wave) can be represented in analog electronics with a voltage. Relatively low frequency signals are considered “baseband” and are very often modulated into high frequency signals for the purpose of effective transmission.

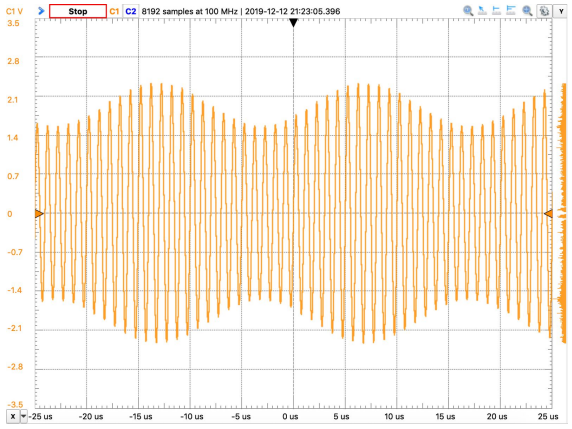

Figure 2: Amplitude Modulation; 1MHz Carrier, 50kHz Data

A cheap and simple, but relatively ineffective way of modulating a data signal into a high-frequency transmission signal is through amplitude modulation (AM). Amplitude modulation is relatively easy to visualize, as both the carrier and the data wave are clearly visible in Figure 2.

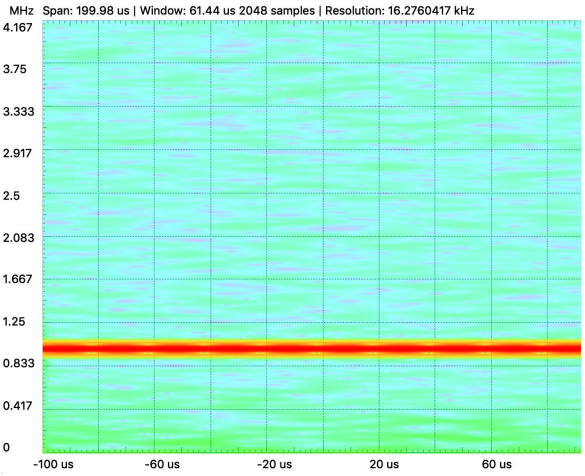

Figure 3: AM Spectrogram; 1MHz Carrier, 50kHz Data

Moving beyond the simplicity of AM, the data can be viewed in a more complex way by applying a Fast Fourier Transform (FFT) to the data, and graphing this FFT over time in what’s known as a spectogram, shown in Figure 3. Note the constant, red signal visible at 1MHz: the carrier frequency. The data signals, once modulated into the AM signal, appear in the frequencies directly above and below the carrier frequency, known as “side bands.” An additional spectrogram for a different AM 200kHz data signal is shown in Figure 4.

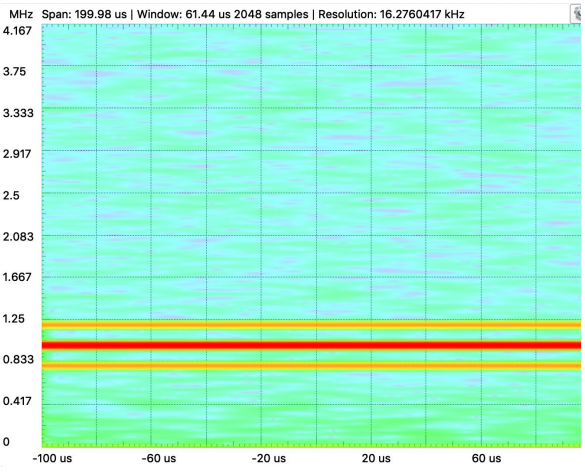

Figure 4: AM Spectrogram; 1MHz Carrier, 200kHz Data

There’s nothing particularly remarkable about the spectrogram for this AM signal, and while we’ve complexified our illustration of the waveform, AM lags behind in complexity. Note how the frequency appears in the

spectrogram: constant through time. The waveform contains the baseband signal in the *amplitude* of the side bands.

Frequency modulation is traditionally more difficult to visualize. You can crank the modulation index up to 50% and try to "imagine" what the frequencies would look like after seeing the time domain (Figure 5), but a spectrogram of an FM waveform reveals far more about the signal.

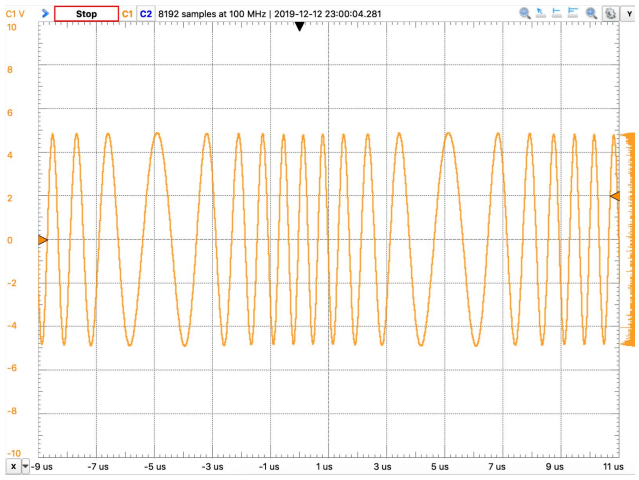

Figure 5: Frequency Modulation; 1MHz Carrier, 100 kHz Signal, 50%

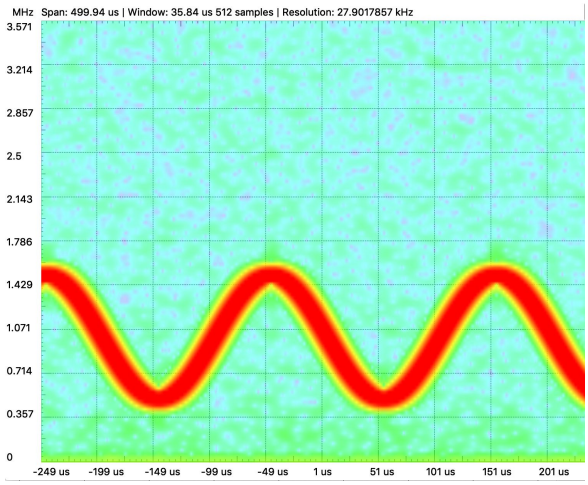

Figure 6: FM Spectrogram; 1MHz Carrier, 5kHz Data, 50%

Notice how we're able to understand a lot more about the FM waveform through the spectrogram. In amplitude modulation, data is encoded in the side bands of the transmission, while in FM, we can see that the frequency of the waveform *itself* encodes the data by oscillating according to the modulation index: 50% illustrated. This is a much more reliable approach, however costing complexity. Because of the intricate nature of an FM signal, more care is required in the demodulation process.

The scope of this project is centered around demodulating an already-modulated FM signal, so the creation of the FM signal will not be discussed. Nevertheless, a firm understanding of the mechanics of frequency modulation is essential to designing a demodulator.

FM Demodulation:

There are several approaches to demodulating an FM signal, but this project focuses on using hardware known as a Phase-Locked Loop (PLL). The PLL is common in many household electronics, and typically appears in FM radio receivers. It consists of a phase detector, a loop filter, and a voltage controlled oscillator.

The input to the PLL is, of course, the FM modulated signal. The output is also the FM modulated signal, which is relatively inconsequential for the purposes of demodulation.

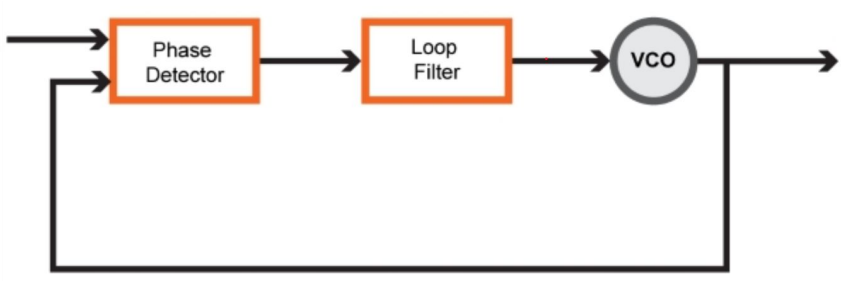

Figure 7: PLL Negative Feedback

VCO: The VCO is an oscillator that should be configured to naturally oscillate at the carrier frequency of the incoming FM wave. By changing the input voltage in the VCO, the output frequency is changed slightly.
Phase Detector: The phase detector takes two inputs: the FM signal and the output from the VCO. The premise behind the phase detector is that a signal is generated proportional to the phase difference of the two incoming waves. The output of the phase detector is filtered, and then applied directly to the VCO.
Loop Filter: Responsible for filtering the output of the phase detector so it's suitable for input into the VCO. The output of this filter is the demodulated signal.

The premise behind the PLL is to take the incoming FM signal and the signal generated by the VCO, and adjust the VCO's output so it exactly matches the incoming FM waveform. As the VCO's output is exactly the same as the FM signal, the input to the VCO must be the modulated data signal

Objectives

- *To study how the Phase-Locked Loop provides feedback to the VCO input.*
- *To study how FM demodulation is achieved.*
- *To study the high-performance nature of the PLL as compared to other FM demodulation techniques.*
- *To develop a complex analog circuit that appears in many household electronics using*
    a. *CD74HC4046A Phase-Locked Loop*
    b. *Passive components*
- *To investigate limitations of the PLL as an FM demodulation tool*

The objective of this project is to design a phase-locked loop (PPL) with the intended application of frequency modulation demodulation. Our team will be using the Texas Instruments CD74HC4046A Phase-Locked Loop with VCO and Lock Detector. This component consists of a phase-locked-loop circuit with a linear voltage-controlled oscillator. The modulated FM signal will be provided by the Digilent Analog Discovery 2. Our phase-locked loop should achieve high-performance FM demodulation. The project will follow the following steps:

- Generate a modulated FM signal with 1MHz carrier and 1kHz (baseband) data at a 20% modulation index
- Create a demodulation circuit using the CD74HC4046A Phase-Locked Loop with VCO and Lock Detector.
- Achieve high-performance FM demodulation with the use of the integrated-circuit PLLs.

The circuit using the CD74HC4046A will consist of:

- A Phase Detector which is a comparator circuit intended to compare input frequency and the VCO output frequency producing a DC voltage that is proportional to the phase difference.
- A Low Pass Filter (LPF) that will be used to greatly reduce the high-frequency components in the output of the phase detector. The LPF also cancels out the high-frequency noise.
- A Voltage Controlled Oscillator (VCO) with the main function of generating an output frequency that is directly proportional to the input voltage.

Challenges

- Create a modulated FM input signal using the Digilent Analog Discovery 2
- Selecting passive components to correctly control the VCO
- Selecting the phase comparator to be used with the VCO
- Designing a Low Pass Filter to be used as the loop filter
- Ensure appropriate feedback path from VCO to phase detector
- Successfully demodulate an FM signal
- Demonstrate the demodulation of that signal using a piezoelectric sensor as a buzzer

Set-up Requirements

Hardware Requirements

- CD74HC4046A Phase-Locked Loop with VCO and Lock Detector.
- Resistors (22k, 100k)
- Capacitors (100pF, 1000pF)
- Piezoelectric transducer to act as a speaker to demonstrate demodulated output (optional)

Block Diagram of PLL Components

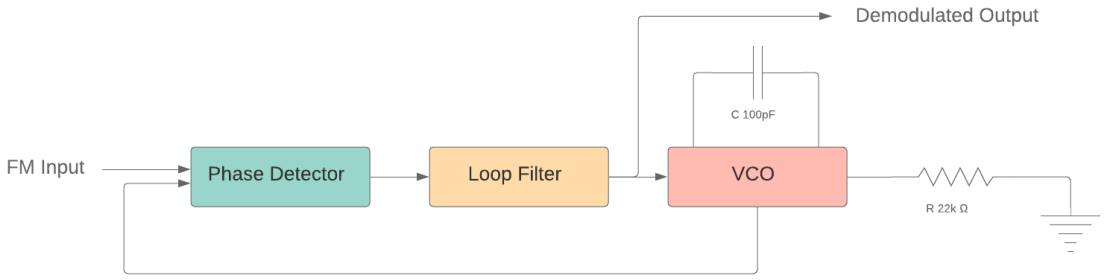

Figure 8: PLL Block Diagram

Multisim PLL Circuit Simulation

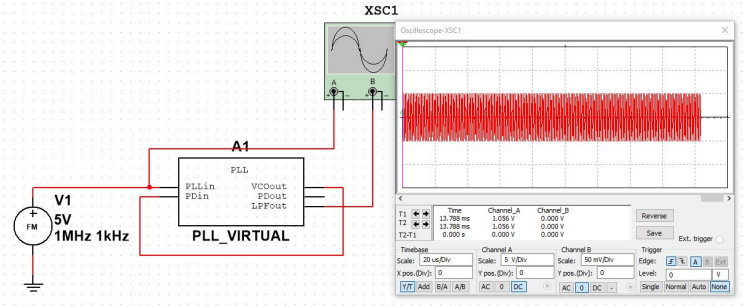

Figure 9: Multisim PLL Simulation Showing Carrier

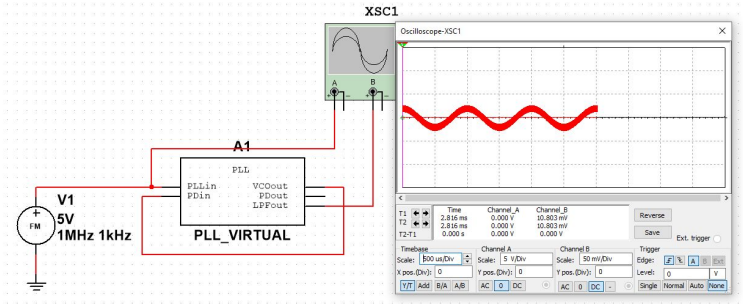

Figure 10: Multisim PLL Simulation Showing Demodulated Output

Hardware Requirements

CD74HC4046A Phase-Locked Loop with VCO and Lock Detector

Features:

- Voltage-controlled oscillator with a high input impedance.
- Phase Comparator 1 which is an Exclusive-OR network
- Phase Comparator 2 which is a positive edge-triggered phase and frequency detector.
- Phase Comparator 3 which is a positive edge-triggered sequential phase detector using an RS-type flip-flop.

Absolute Maximum Ratings;

- DC Supply Voltage (VCC): -0.5V to 7V
- DC Input Diode Current (IIK) For VI < -0.5V or VI > VCC + 0.5V: ±20mA
- DC Output Diode Current (IOK) For VO < -0.5V or VO > VCC + 0.5V: ±20mA DC
- Drain Current, per Output IO For -0.5V < VO < VCC + 0.5V: .±25mA
- DC Output Source or Sink Current per Output Pin, IO For VO > -0.5V or VO < VCC + 0.5V: .±25mA
- DC VCC or Ground Current (ICC): ±50mA

CD74HC4046A Connection Information:

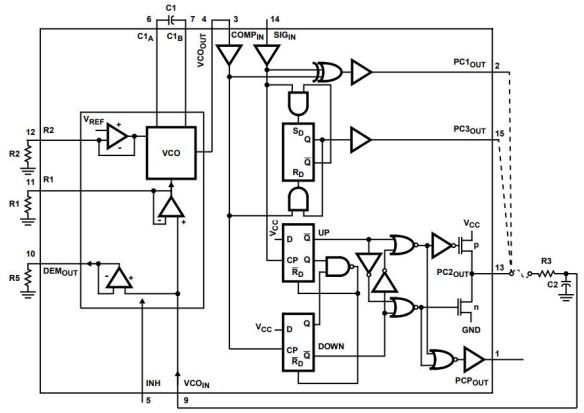

Figure 11: CD74HC4046A Schematic Diagram

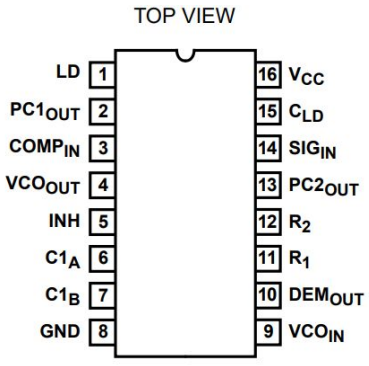

Figure 12: CD74HC4046A Pinout

Component Configuration

The datasheet for the PLL provides a general connection strategy. The device provides the choice between three different phase comparators. For the purposes of this project, Phase Comparator 1 will be used. Components R3, R4, and C2 are part of the low pass filter, which will be discussed shortly. The output of the filter is fed to VCO_IN. The VCO is configured using C1, R1, and R2 as specified in the datasheet.

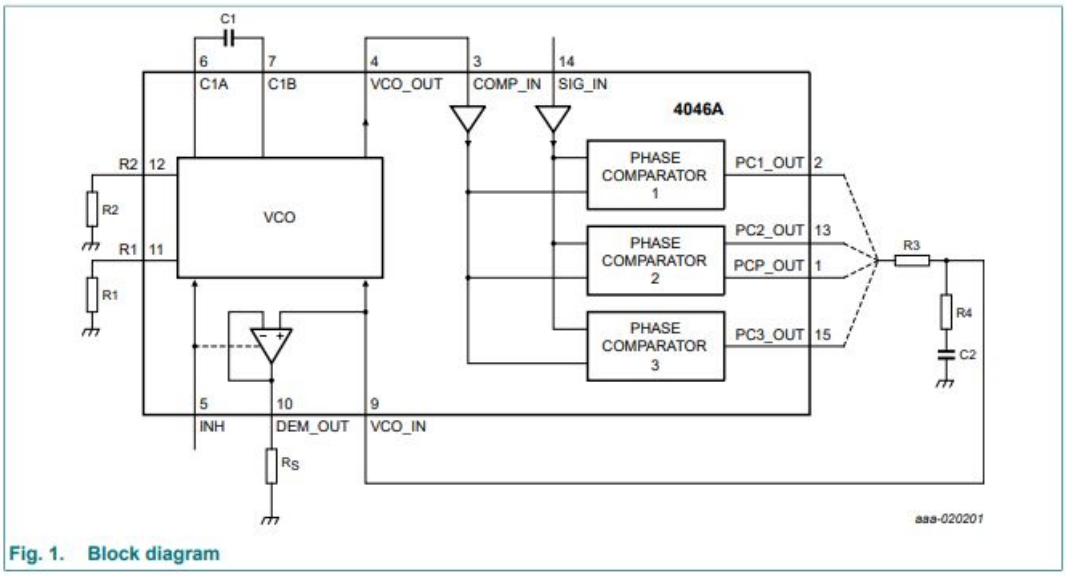

Figure 13: General PLL Connection Strategy

Selection of R1 and C1

The datasheet provides some insight as to the choice of R1 and C1 in order to choose the VCO's center frequency. The datasheet indicates that for maximum stability, C1 can be selected to be 100pF. To achieve the VCO center frequency of 1MHz, the resistor value R1 is interpolated to find the correct value. This interpolation process is described more in depth.

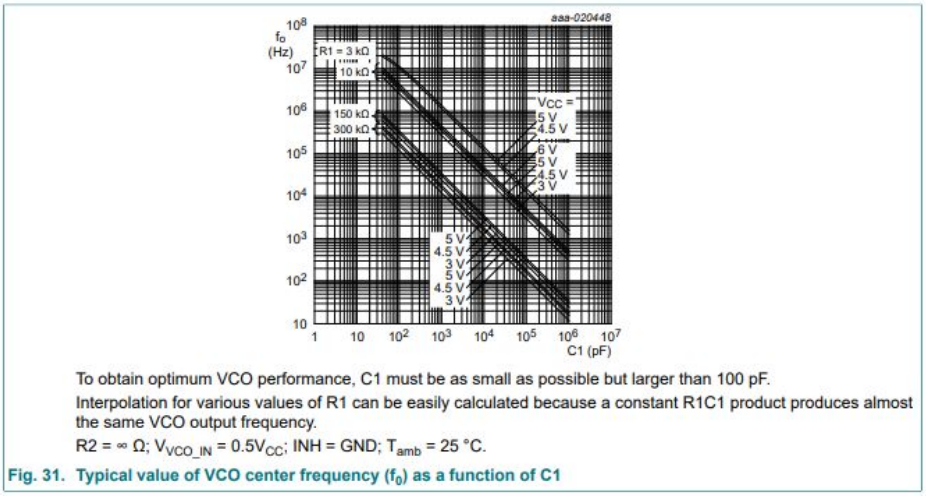

Figure 14: PLL R1 and C1 Selection

As shown in Figure 15, the datasheet indicates that the frequency increase is relatively linear. Figure 14 allows us to interpolate a resistor value R1 that centers the VCO frequency at 1MHz.

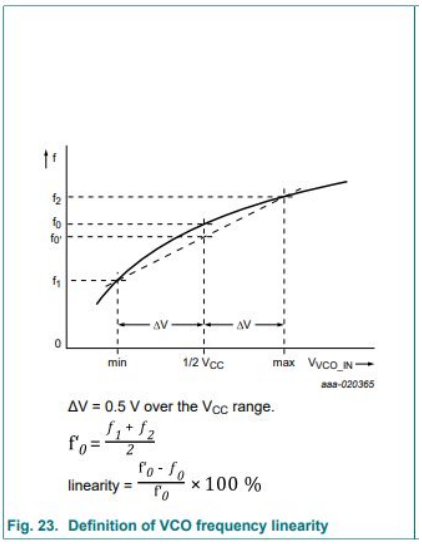

Figure 15: VCO Frequency Linearity

With the center frequency at 10 MHz, R1 is found to be 3k. With the center frequency at 1.1 kHz, R1 is found to be 300k. Using interpolation, for a frequency of 1MHz, resistor 1 should be selected to be approximately 15k. Due to material availability, a 22k resistor will be used.

The datasheet also describes the functionality of R2. R2 allows for frequency offset to be applied to the FM demodulation. Since the modulated signal in this project is a baseband signal, no frequency offset will be applied. With no frequency offset, R2 is selected to be infinite impedance, and is left open. Finally, Rs is selected to be 100k to apply load to the DEM_OUT pin per the datasheet.

Selection of Low Pass Filter

The datasheet also provides significant information on Low Pass Filter selection.

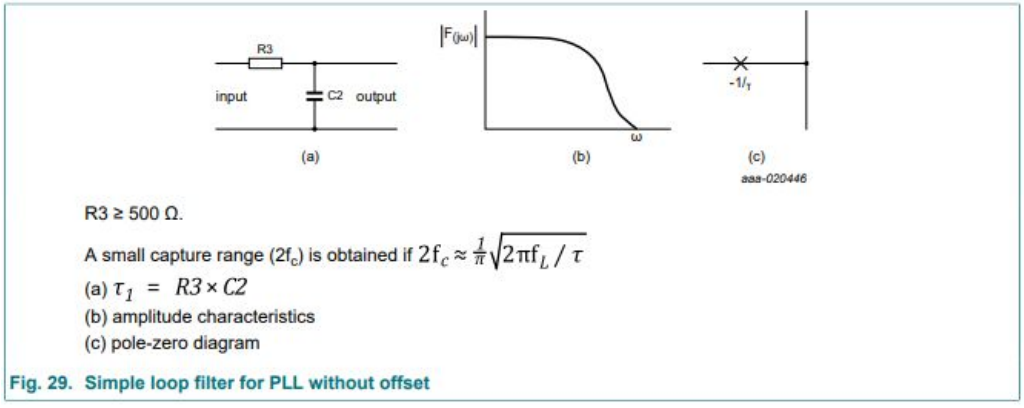

Figure 16: Low Pass Filter Component Selection

The low pass filter is responsible for filtering the input into the VCO, which should look identical to the original modulated input frequency. In this project, baseband signals will be modulated into the carrier frequency, and there can be reasonable confidence that the modulated signal will never exceed 10kHz. As such, a capture frequency, $2f_C$ of 10kHz will be selected for the low pass filter.

The datasheet guides the math on resistor and capacitor selection. Due to component availability, a 1000pF capacitor will be used. The capture frequency $2f_C$ will be set as 10kHz, and the lock frequency is determined by the modulation index of the input signal. For this project, a modulation index of 20% will be used. The lock frequency is also determined by the datasheet, and is set at 5000 Hz. The time constant tau can be calculated using their given equation, and used to select the resistor.

$$2f_C = \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau}}$$

$$\frac{(10kHz * \pi)^2}{2\pi\,(5000\ Hz)} = \frac{1}{\tau}$$

$$\tau = 3.183 * 10^{-5}$$

$$\tau = R * C$$

$$3.183 * 10^{-5} = R * (1000\ pF)$$

$$R = 31.8k\ \Omega$$

Due to component availability, the capture frequency of the low pass filter will be increased slightly so a 22k resistor can be used. The low pass filter, using a 1000pF capacitor and a 22k resistor, was simulated in multisim to ensure the correct frequencies are removed.

Low Pass Filter Multisim Simulation

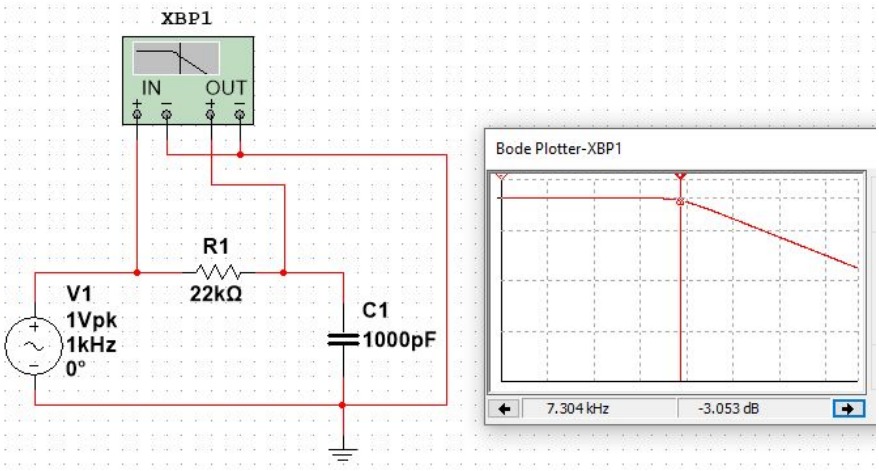

Figure 17: Low Pass Filter Simulation and Bode Plot

The final design of the circuit follows the block diagram specified in the datasheet. Passive components are added to configure the device. The center frequency, f_C is set at 1MHz. The lock frequency, $2f_L$ is set to the modulation index, 20% of the carrier frequency, or 10kHz. With all components of the device selected, the PLL can be tested with an FM waveform from the Analog Discovery 2.

Device Testing

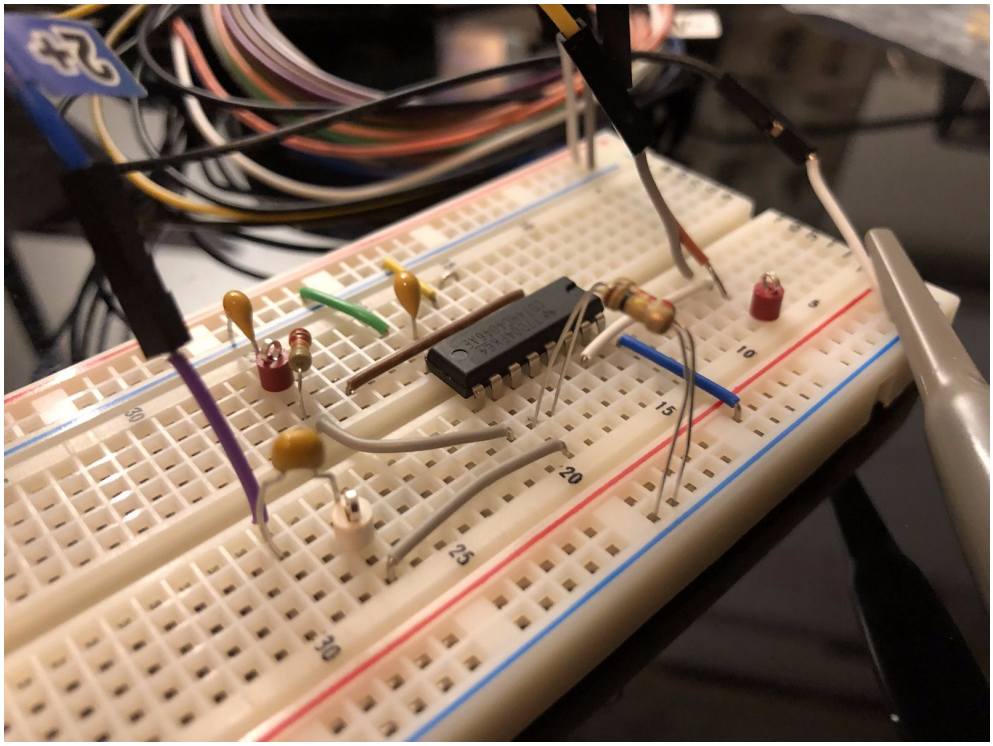

Figure 18: Breadboarded FM Demodulation Device

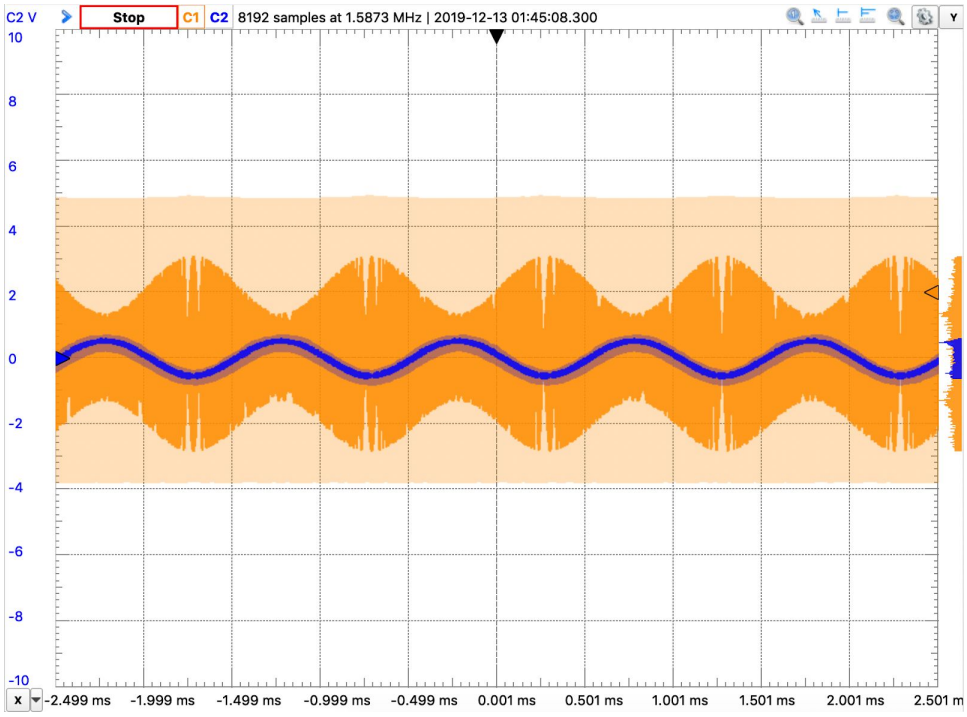

Figure 19: FM Demodulated Output Shown in Blue, FM Input in Orange

The device is run with several baseband data frequencies modulated into a 1MHz carrier wave. As long as the data signal is low frequency enough to pass through the low pass filter, the device is successfully able to demodulate various FM signals. Several demodulated outputs are shown below:

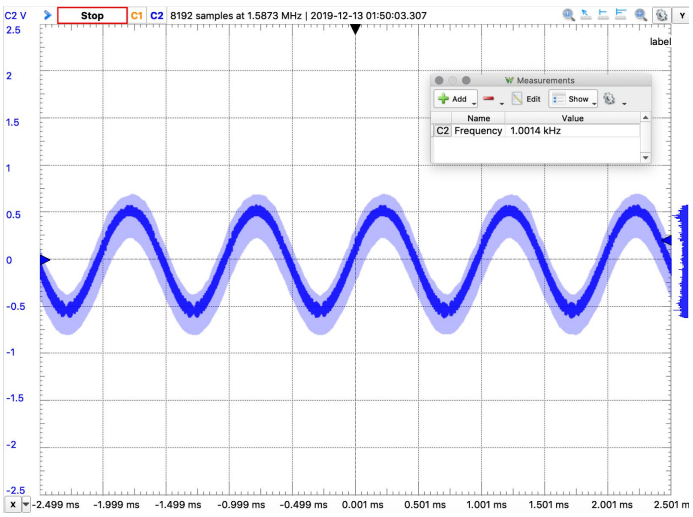

Figure 20: Demodulated 1kHz Signal

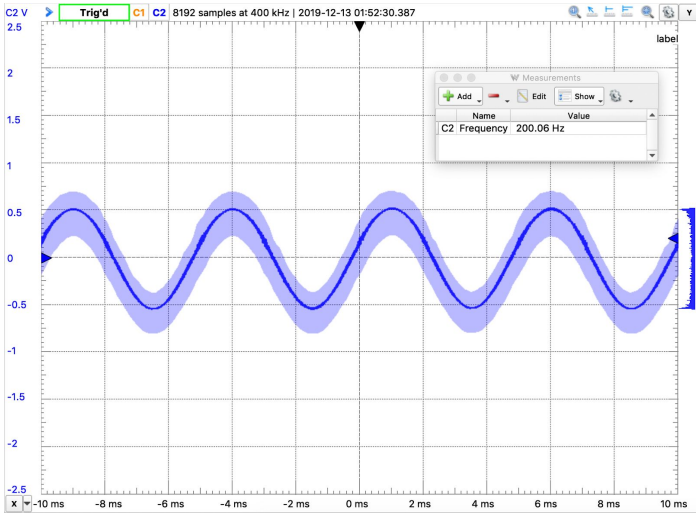

Figure 21: Demodulated 200Hz Signal

Conclusion

The objective of this project was to explore one of several methods of demodulating an FM waveform. The strategy attempted here uses a closed-feedback system known as a Phase-Locked Loop to generate a new signal with the same frequency as the original frequency-modulated input. In this process, an identical FM waveform is generated, but the input into the VCO for creating this waveform can be directly accessed as the demodulated data signal. The result of this strategy was successful, and baseband signals less than 10kHz can be robustly demodulated using the hardware demonstrated in this project.

Appendix: Images

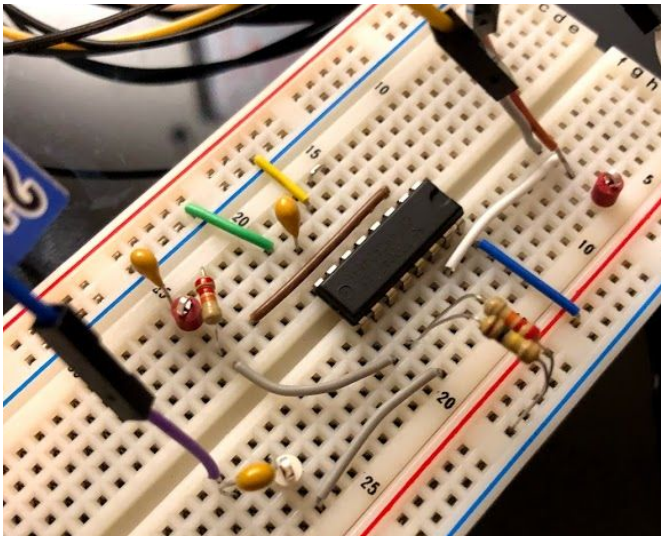

Figure 22: Breadboarded PLL Circuit

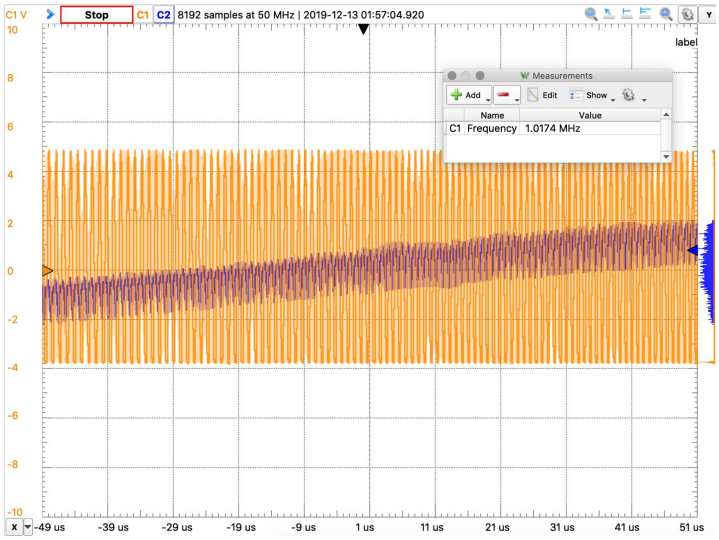

Figure 23: Close-up of FM Modulated Signal (Orange)

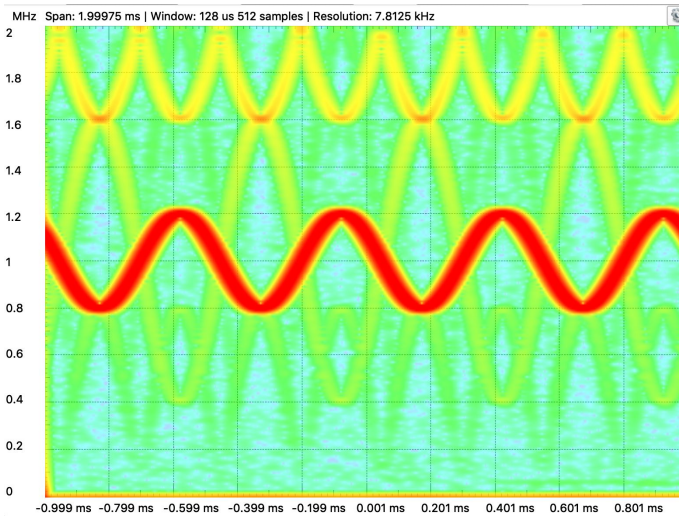

Figure 24: Spectrogram of Modulated 2kHz Data Signal

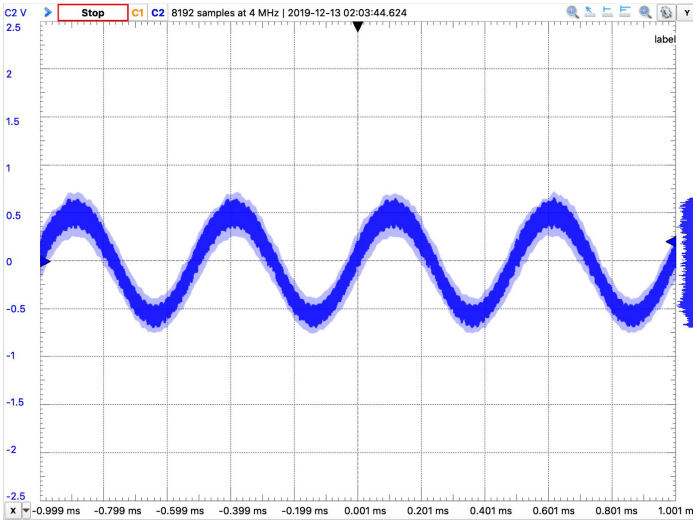

Figure 25: Demodulated PLL Output of 2kHz Data Signal

Appendix: Circuit Diagram

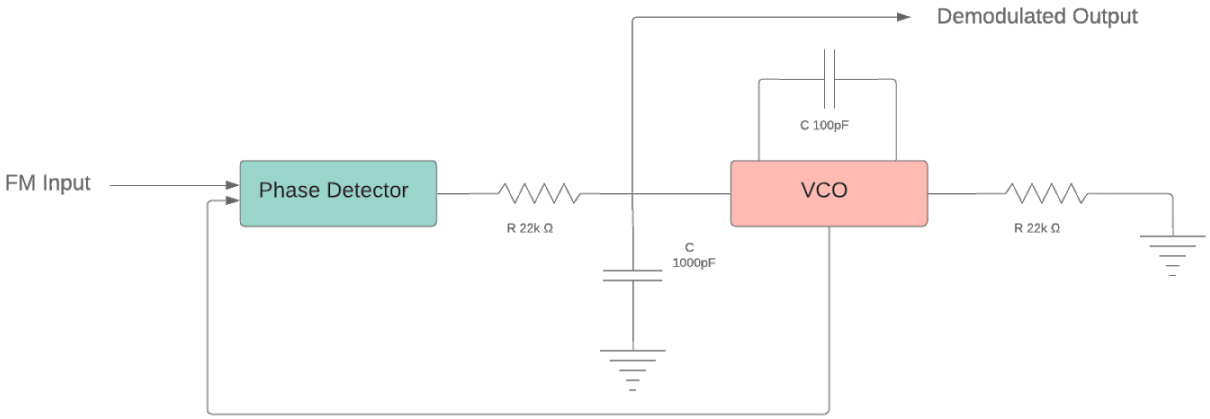

Figure 26: Circuit Diagram of PLL Demodulator

References

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[3] “Phase Locked Loops, block diagram,working,operation,Design,Applications,” *Electronic Circuits and Diagrams-Electronic Projects and Design*, 24-Jan-2018. [Online]. Available: http://www.circuitstoday.com/pll-phase-locked-loops. [Accessed: 13-Dec-2019].

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Datasheets

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Example circuit

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